Spread Spectrum Clock Generator

This application is a Continuation-In-Part of U.S. Serial No. 10/647,929 entitled "Spread Spectrum Clock Generator" filed August 26, 2003, which is incorporated by reference in its entirety, herein.

Background of the Invention

The subject application is directed generally to the art of synchronous digital circuitry, and more particularly to synchronous digital circuitry in which a lessened effect of electromagnetic interference ("EMI") is desirable.

Most digital devices today operate synchronously. That is, data processing operations occur under a timing dictated by a digital clock signal. Such digital clock signals are typically square waves that oscillate at a selected frequency. As improvements are made to digital processing devices, clock frequencies may be increased. Faster clock frequencies allow for improved data processing throughput. Current digital clock frequencies are already in the multi-gigahertz range. As clock frequencies continue to rise, an increased incidence of electromagnetic interference exists. Such EMI requires that special shielding or casing be developed to dampen such interference. EMI can cause data errors in associated data processing devices, as well as provide for radio frequency ("RF") interference for analog devices such as radios and televisions.

Designers have become aware that implementing a spread spectrum clock generator ("SSCG") works to substantially reduce the high energy spikes associated with digitally-generated EMI.

SSCG circuitry functions to vary slightly a frequency of a digital clock signal over time. This is accomplished by reducing "noise" associated with harmonics of a large scale integration ("LSI") clock signal. SSCG circuitry functions to alter slightly a signal interval and thus diffuses a frequency spectrum and lowers a peak value.

A side effect from the use of an SSCG is an introduction of a slight jitter in the system clock. However, such jitter is generally of little consequence other than in

particular applications relating to communication network interfaces or input/output interfaces, as well as other applications having varying tolerance to jitter. Thus, it is desirable to be able to vary a degree of frequency shift and associated jitter to accommodate a lessening of peak EMI while simultaneously minimizing the jitter to acceptable application parameters.

Current SSCG circuitry employs frequency comparators and voltage controlled oscillators ("VCO") to accomplish the shifting of frequency to result in a modulated clock signal. While effective, such analog-based implementations render it difficult and expensive to accomplish an SSCG circuitry, particularly in applications when a system is desired to coexist on other standard digital circuitry and in conjunction with a single substrate.

The subject invention provides for a digital spread spectrum clock generator which accomplishes selected frequency variation of an associated digital clock while minimizing the required use of extensive or incompatible analog circuitry.

Summary of the Invention

In accordance with the subject invention, there is provided a spread spectrum clock generator which includes a divider for lowering a frequency of an input clock signal. A digital counter is incremented synchronously with the clock signal. The counter, in turn, processes through a selected sequence of outputs to be generated by a pattern generator. The pattern generator output, in turn, is communicated to a digitally controllable delay circuit into which the lowered frequency clock signal is provided. Thus, a variation in frequency to the clock signal is controlled by the selected pattern in the pattern generator. This varying frequency clock signal is then multiplied to a higher overall frequency compatible with the original clock signal, and output as a clock signal to remaining, synchronous digital circuitry.

In accordance with another aspect of the present invention, the frequency variation of the modified clock signal is toggled between a selected higher limit and selected lower limit.

In accordance with another aspect of the present invention, a method is provided for generating a spread spectrum clock signal in accordance with the foregoing.

Summary of the Drawings

The subject invention is described with reference to certain parts, and arrangements to parts, which are evidenced in conjunction with the associated drawings which form a part hereof and not for the purposes of limiting the same in which:

Fig. 1 is a schematic of a conventional spread spectrum clock generator;

Fig. 2 is a diagram of the improved spread spectrum clock generator of the present invention;

Fig. 3 is a block diagram of the spread spectrum clock generator of the subject invention inclusive of a master clock, the frequency of which is lowered prior to alteration of a frequency and raised after completion thereof;

Fig. 4 is a diagram of the input clock wave form as compared to the output clock which has been processed for spread spectrum frequency modulation; and

Fig. 5 is a graph of clock period versus frequency delta associated with the spread spectrum clock generation of the subject invention.

Fig. 6 is a diagram of an integrated circuit of the present invention.

Fig. 7 is a diagram of used delay line circuit.

Fig. 8a and Fig. 8b illustrate the difference between "Phase Modulation" and "Frequency Modulation" based on the modulation pattern difference.

Fig. 9a and 9b illustrate an example of "Phase Modulation Pattern" and its result waveform.

Fig. 10a and 10b illustrate an example of "Frequency Modulation Pattern" based on this invention and its result waveform.

Fig. 11 shows an integrated circuit of the present invention with external peripheral devices such as ATA100, PCI Controller.

Fig. 12 shows the contents of pattern generator, which modulates 20 MHz source clock used in a particular application.

Fig. 13 shows the modulation waveform in the example of Fig. 12 pattern table.

Detailed Description of the Preferred Embodiment

Turning now to the drawings wherein the illustrations are for illustrating the preferred embodiment only, and not for delivering the same, Fig. 1A shows a block diagram of a conventional spread spectrum clock generator. In a conventional system, a clock input 10 was provided as one input to a frequency phase comparator 12. An output of the comparator 12 was provided to a charge pump 14, the output of which is provided to a voltage controlled oscillator ("VCO 16"). Output 18 of the VCO 16 forms a system clock output, as well as a feedback loop into frequency comparator 12 via a 1/N divider 20.

A conventional spread spectrum clock generator employed an RC circuit 22 as a filter to ground. A signal generator 24 served to generate a waveform (such as that evidenced in Fig. 1B) into the input of the VCO 16. By injecting this signal into the VCO input, an output frequency at output 18 was modulated in conjunction with the waveform of Fig. 1B.

It will be appreciated by the view of Figs. 1A and 1B that the basic circuitry employed in the spread spectrum clock generator was that of a phase lock loop. The system, while functional, relied heavily on analog circuitry and was thus not readily adaptable to implementation in conjunction with digital circuitry.

Turning now to Fig. 2, the basic architecture of the spread spectrum clock generator of the present invention is described. The SSCG A includes a clock input 30, which input is provided by the standard clock generated in conjunction with a frequency associated with an associated synchronous digital system. The clock input from 30 is communicated to an input 32 of a digital delay line 34. The input 30 is also communicated to an input 36 of a counter 38. The counter 38 is suitably comprised of any simple binary counter. In the preferred embodiment, the counter 38 functions to count an increment on the basis of a number of input clock signals generated at counter input 36.

The counter 38 is in data communication with the pattern generator 40 through its output lines thereof (not shown). In a simple binary counter, a series of binary lines are provided which correspond to a base numeric sequence. In a preferred embodiment, a

particular binary number placed on an input to the pattern generator results in the providing of a preselected digital value at an output 50 thereof. A particular pattern of a pattern generator 40 of the preferred embodiment will be detailed in conjunction with Table 1, below. In the preferred embodiment, sequencing the counter 38 will result in a periodically repeating pattern being generated by pattern generator 4 at output 50.

Table 1 The TRUTH table of Pattern Generator

S	D	V	S	D	V	S	D	V	S	D	V	S	D	V	S	D	V	S	D	V	S	D	V	S	D	V	S	D	V
0	0	16	60	1	61	120	3	191	180	3	376	240	1	478	300	0	493	360	-2	423	420	-4	265	480	-2	98	540	-1	23
1	0	16	61	2	63	121	3	194	181	2	378	241	1	479	301	-1	492	361	-2	421	421	-4	261	481	-2	96	541	0	23
2	0	16	62	1	64	122	2	196	182	3	381	242	1	480	302	0	492	362	-1	420	422	-3	258	482	-2	94	542	-1	22
3	1	17	63	2	66	123	3	199	183	2	383	243	0	480	303	-1	491	363	-2	418	423	-4	254	483	-1	93	543	0	22
4	0	17	64	1	67	124	3	202	184	2	385	244	1	481	304	0	491	364	-2	416	424	-4	250	484	-2	91	544	-1	21
5	0	17	65	2	69	125	3	205	185	3	388	245	1	482	305	-1	490	365	-2	414	425	-4	246	485	-2	89	545	0	21
6	0	17	66	1	70	126	3	208	186	2	390	246	1	483	306	0	490	366	-2	412	426	-4	242	486	-2	87	546	-1	20
7	0	17	67	2	72	127	3	211	187	2	392	247	1	484	307	-1	489	367	-2	410	427	-4	238	487	-2	85	547	0	20
8	1	18	68	1	73	128	4	215	188	2	394	248	0	484	308	0	489	368	-2	408	428	-3	235	488	-1	84	548	-1	19
9	0	18	69	2	75	129	3	218	189	3	397	249	1	485	309	-1	488	369	-3	405	429	-4	231	489	-2	82	549	0	19
10	0	18	70	2	77	130	3	221	190	2	399	250	1	486	310	-1	487	370	-2	403	430	-3	228	490	-2	80	550	0	19
11	0	18	71	1	78	131	3	224	191	2	401	251	1	487	311	0	487	371	-2	401	431	-4	224	491	-2	78	551	-1	18
12	1	19	72	2	80	132	4	228	192	2	403	252	0	487	312	-1	486	372	-2	399	432	-3	221	492	-1	77	552	0	18
13	0	19	73	2	82	133	3	231	193	2	405	253	1	488	313	-1	485	373	-2	397	433	-3	218	493	-2	75	553	0	18
14	0	19	74	2	84	134	4	235	194	3	408	254	1	489	314	-1	484	374	-3	394	434	-3	215	494	-2	73	554	0	18
15	1	20	75	1	85	135	3	238	195	2	410	255	0	489	315	0	484	375	-2	392	435	-4	211	495	-1	72	555	-1	17
16	0	20	76	2	87	136	3	241	196	2	412	256	1	490	316	-1	483	376	-2	390	436	-3	208	496	-2	70	556	0	17
17	1	21	77	2	89	137	4	245	197	2	414	257	0	490	317	-1	482	377	-2	388	437	-3	205	497	-1	69	557	0	17
18	0	21	78	2	91	138	4	249	198	2	416	258	1	491	318	-1	481	378	-3	385	438	-3	202	498	-2	67	558	0	17
19	1	22	79	2	93	139	4	253	199	2	418	259	0	491	319	-1	480	379	-2	383	439	-3	199	499	-1	66	559	0	17
20	0	22	80	1	94	140	3	256	200	2	420	260	1	492	320	0	480	380	-2	381	440	-3	196	500	-2	64	560	-1	16
21	1	23	81	2	96	141	4	260	201	1	421	261	0	492	321	-1	479	381	-3	378	441	-2	194	501	-1	63	561	0	16
22	0	23	82	2	98	142	4	264	202	2	423	262	1	493	322	-1	478	382	-2	376	442	-3	191	502	-2	61	562	0	16
23	1	24	83	2	100	143	4	268	203	2	425	263	0	493	323	-1	477	383	-3	373	443	-3	188	503	-1	60	563	0	16
24	0	24	84	2	102	144	4	272	204	2	427	264	1	494	324	-1	476	384	-2	371	444	-3	185	504	-2	58			
25	1	25	85	2	104	145	4	276	205	2	429	265	0	494	325	-1	475	385	-3	368	445	-3	182	505	-1	57			
26	0	25	86	2	106	146	3	279	206	1	430	266	1	495	326	-1	474	386	-2	366	446	-2	180	506	-2	55			
27	1	26	87	3	109	147	4	283	207	2	432	267	0	495	327	-2	472	387	-3	363	447	-3	177	507	-1	54			
28	1	27	88	2	111	148	3	286	208	2	434	268	0	495	328	-1	471	388	-2	361	448	-3	174	508	-1	53			
29	0	27	89	2	113	149	4	290	209	2	436	269	1	496	329	-1	470	389	-3	358	449	-3	171	509	-2	51			
30	1	28	90	2	115	150	3	293	210	1	437	270	0	496	330	-1	469	390	-2	356	450	-2	169	510	-1	50			
31	1	29	91	2	117	151	3	296	211	2	439	271	0	496	331	-1	468	391	-3	353	451	-3	166	511	-1	49			
32	1	30	92	3	120	152	3	299	212	2	441	272	0	496	332	-2	466	392	-2	351	452	-3	163	512	-1	48			
33	0	30	93	2	122	153	4	303	213	1	442	273	1	497	333	-1	465	393	-3	348	453	-2	161	513	-2	46			
34	1	31	94	2	124	154	3	306	214	2	444	274	0	497	334	-1	464	394	-3	345	454	-3	158	514	-1	45			
35	1	32	95	2	126	155	3	309	215	1	445	275	0	497	335	-1	463	395	-2	343	455	-2	156	515	-1	44			
36	1	33	96	3	129	156	3	312	216	2	447	276	0	497	336	-2	461	396	-3	340	456	-3	153	516	-1	43			
37	1	34	97	2	131	157	3	315	217	1	448	277	0	497	337	-1	460	397	-3	337	457	-2	151	517	-1	42			
38	0	34	98	2	133	158	3	318	218	2	450	278	1	498	338	-1	459	398	-3	334	458	-3	148	518	-2	40			
39	1	35	99	3	136	159	2	320	219	1	451	279	0	498	339	-2	457	399	-2	332	459	-2	146	519	-1	39			
40	1	36	100	2	138	160	3	323	220	2	453	280	0	498	340	-1	456	400	-3	329	460	-3	143	520	-1	38			
41	1	37	101	3	141	161	3	326	221	1	454	281	0	498	341	-2	454	401	-3	326	461	-2	141	521	-1	37			
42	1	38	102	2	143	162	3	329	222	2	456	282	0	498	342	-1	453	402	-3	323	462	-3	138	522	-1	36			
43	1	39	103	3	146	163	3	332	223	1	457	283	0	498	343	-2	451	403	-3	320	463	-2	136	523	-1	35			
44	1	40	104	2	148	164	2	334	224	2	459	284	0	498	344	-1	450	404	-2	318	464	-3	133	524	-1	34			
45	2	42	105	3	151	165	3	337	225	1	460	285	-1	497	345	-2	448	405	-3	315	465	-2	131	525	0	34			
46	1	43	106	2	153	166	3	340	226	1	461	286	0	497	346	-1	447	406	-3	312	466	-2	129	526	-1	33			
47	1	44	107	3	156	167	3	343	227	2	463	287	0	497	347	-2	445	407	-3	309	467	-3	126	527	-1	32			
48	1	45	108	2	158	168	2	345	228	1	464	288	0	497	348	-1	444	408	-3	306	468	-2	124	528	-1	31			
49	1	46	109	3	161	169	3	348	229	1	465	289	0	497	349	-2	442	409	-3	303	469	-2	122	529	-1	30			
50	2	48	110	2	163	170	3	351	230	1	466	290	-1	496	350	-1	441	410	-4	299	470	-2	120	530	0	30			
51	1	49	111	3	166	171	2	353	231	2	468	291	0	496	351	-2	439	411	-3	296	471	-3	117	531	-1	29			
52	1	50	112	3	169	172	3	356	232	1	469	292	0	496	352	-2	437	412	-3	293	472	-2	115	532	-1	28			
53	1	51	113	2	171	173	2	358	233	1	470	293	0	496	353	-1	436	413	-3	290	473	-2	113	533	-1	27			
54	2	53	114	3	174	174	3	361	234	1	471	294	-1	495	354	-2	434	414	-4	286	474	-2	111	534	0	27			
55	1	54	115	3	177	175	2	363	235	1	472	295	0	495	355	-2	432	415	-3	283	475	-2	109	535	-1	26			
56	1	55	116	3	180	176	3	366	236	2	474	296	0	495	356	-2	430	416	-4	279	476	-3	106	536	-1	25			
57	2	57	117	2	182	177	2	368	237	1	475	297	-1	494	357	-1	429	417	-3	276	477	-2	104	537	0	25			
58	1	58	118	3	185	178	3	371	238	1	476	298	0	494	358	-2	427	418	-3	273	478	-2	102	538	-1	24			
59	2	60	119	3	188	179	2	373	239	1	477	299	-1	493	359	-2	425	419	-4	269	479	-2	100	539	0	24			

As will be appreciated by one of ordinary skill in the art, a feed digital delay line 34 functions to provide a selected delay to an input signal, the duration of which delay is dictated by an input thereto such is provided by the output of pattern generator 50. Thus, a clock signal 30 will be provided with a selected delay, as dictated by the output of the

pattern generator 40, and this delay will be provided on output 52. It will be appreciated, therefore, that interaction between the counter 38, pattern generator 40 and digital delay line 34 will serve to provide a selected delay sequence to respective pulses of the clock signal at input 30, as it is output to output 52. In this fashion, the entire sequence of delay is suitably fabricated from digital elements and avoids implementation of the VCO/PLL circuitry as provided in connection with Fig. 1A, above.

Turning now to Fig. 3, the SSCG A of Fig. 1A is shown in connection with additional support circuitry. Conventional switching circuitry currently operates in the multi-gigahertz range. It will be appreciated that implementation of the counter, pattern generator and digital delay line, such as described herein, is more readily adapted to perform at lower frequencies than this. The additional structure of Fig. 3 accomplishes the beneficial advantages of the subject invention while facilitating use in connection with substantially higher clock frequencies. An input from a master clock 60 has communicated to a divider 62 to divide the frequency thereof. In the preferred embodiments, divider 62 is a 1/3 divider. By way of example, an input master clock frequency of 48 MHz provided at input 60 would result in a 16MHz signal being provided at the output of divider 62, which forms the clock input 30. Thus, a period of 20.83 microseconds can be extended to a period of 62.5 microseconds. The function of the SSCG A is as described in connection with Fig. 2, above.

Turning now to the output 52 of digital delay line 34 in Fig. 3, in this embodiment the output forms an input to a phase lock loop 70. As will be appreciated by one of ordinary skill in the art, the PLL 70 suitably serves as a signal conditioner to clean an output pulse, as well as a system for stepping up an input frequency. The PLL 70 suitably takes an input of 16 MHz, as provided from the output 52 of the digital delay line 34, and outputs a substantially higher frequency, 400 MHz in the preferred embodiment and which output is provided at 72. Also, an internal divider 74 suitably provides feedback at terminal 76 to allow for the enhanced output at 72.

Turning now to Fig. 4, a comparison of an input clock and an output clock 82 is described as a function of time. The input clock shows a suitable system clock input, such as may be provided at digital delay line input 30 (Fig. 1A) or master clock input 60

(Fig. 2). An output waveform 82 evidences a skew in frequency as provided by the SSCG circuitry described above.

Turning now to Table 1, disclosed is a suitable true table of the content of a pattern generator such as described herein. In the preferred embodiment, the decoder content of the subject invention will be applied with every 564 clock cycles. In this fashion, a modulation frequency of around 28 KHz is provided. As used in Table 1, S refers to "step", D "delay value", and V refers to "decoder value". The step value S is incremented with every input clock pulse, such as that provided at input 30 (Fig. 1A or Fig. 2). A specified delay value and decoder value follows every increment of the counter 38. While the values of Fig 1A are provided in the preferred embodiment, it will be appreciated that other suitable values may be implemented to accomplish the delays of the subject invention.

Turning now to Table 2, an example output of the pattern generator 40 is detailed. As evidenced in Table 2, the counter will increment at every input clock. At such point as a counter shows a value of 16, the next value will be reset to a 0. Thus, the pattern generator will decode a counter value to appear in the column "Pattern" and feed it to the delay line (50) (Figs. 2 and 3). As noted above, the delay line 34 will delay an input clock by the value given from its input 50. By way of example, when a counter value is set at 0, delay value is 0. When a counter achieves 1, the delay is 1. Next, the delay value will skip 1 and the result will be 3. As evidenced in Fig. 2, the values of column DELTA P show the difference between each adjacent account. This sequence of delta values, up and down in the preferred embodiment, is evidenced therein.

Table 2 Example of pattern generator table

Count	Pattern	DELTA T	Delta T
0	0	0	0.00%
1	1	1	0.05%
2	3	2	0.10%
3	6	3	0.15%
4	10	4	0.20%
5	13	3	0.15%
6	15	2	0.10%
7	16	1	0.05%
8	16	0	0.00%
9	15	-1	-0.05%
10	13	-2	-0.10%
11	10	-3	-0.15%
12	6	-4	-0.20%
13	3	-3	-0.15%
14	1	-2	-0.10%
15	0	-1	-0.05%

Referring back to Fig. 3, when an input to the SSCG A is at a value T, a first period and its corresponding output is T1-T0, which is T+Δ. As used herein, Δ is a unidelay of the delay line. As used herein:

$$
\begin{aligned}
&T1\text{-}T0 = T + \Delta \\
&T2\text{-}T1 = T + 2 * \Delta \\
&T3\text{-}T2 = T + 3 * \Delta \\
&T4\text{-}T3 = T + 4 * \Delta \\
&T5\text{-}T4 = T + 3 * \Delta
\end{aligned}
$$

As shown in the above, the frequency modulation can be achieved because the period during each clock cycle is changed.

Turning now to Fig. 5, discloses a graph evidencing the frequency modulation scheme of the preferred embodiment. With the implementation described in the preferred embodiment, detailed above, it will be appreciated that the frequency modulation scheme employed by the circuitry of the subject invention provides for modulation analogous to that provided in conventional circuitry, as evidenced by Fig. 1B. Thus, the subject system provides for spread spectrum clock generation so as to provide all the advantages of the earlier system, but in a substantially improved, digital structure that is readily adaptable to integration and low cost and effective applications.

Fig. 6 shows, as an example, of a diagram of an integrated circuit of the present invention. An integrated circuit 100 includes an SSCG 110 of the preset invention and a microprocessor 120. The SSCG 110 receives a constant clock (A) and provides a varying frequency clock (B) to the microprocessor 120. The microprocessor 120 includes at least a program counter 121, an instruction fetch unit 122, an instruction decoder 123, and an execution unit 124. The program counter 121 increments its stored value in response to the varying frequency clock. The microprocessor 120 can be either of a Reduced Instruction Set Computer ("RISC"), Complex Instruction Set Computer ("CISC"), or a Very Long Word Instruction computer ("VLIW"). A center frequency of the varying frequency clock to the microprocessor is, preferably, from 300MHz to 900MHz.

The integrated circuit shown in Fig. 6 can be manufactured by a semiconductor process technology with a design rule of 0.13um or less. In other words, a gate length of

a transistor element is of 0.13um or less. The design rule of less than 0.1um can be used employed, too. Further, copper can be used for an interconnection or wiring of the integrated circuit.

Fig. 7 shows a diagram of the digital delay line 34 of the present invention. The digital delay line includes a plurality of delay elements (341), a one-hot decoder (343), and a set of delay value input (342), in response to the output of the decoder 40. Each of the delay elements consists of three NAND gates and it has clock injection input (344). The source clock will be injected in to the point where the rest of delay elements numbers is corresponding to the delay value. Because of this structure, the delay value input can be changed whenever the input clock is low level without hazard.

Earlier Systems allowed on circuit to generate "phase modulated" waveform if the content of pattern generator designed as such. Fig. 8a shows an example of an earlier "Phase Modulation" system. On the other hand, Fig. 8b shows the case of "Frequency Modulation" as is described herein.

Fig 9a shows an example of "phase modulation pattern". By using this pattern, the output clock shows triangle waveform in its phase domain and square waveform in its frequency domain. From the spread spectrum viewpoint, this frequency spectrum is split to two frequencies, such as f0+Delta and f0-Delta. This result is shown in Fig. 9b.

Fig. 10a is an example of "Frequency Modulation pattern" based on this invention. The result is shown in Fig. 10b, where the phase modulation waveform is "integral waveform", which is resemble to Sine wave.

As illustrated in Fig. 8b, a clock input is received at terminal 400. A received clock signal is provided as an input a phase shifter 402. The phase shifter 402, in turn, receives frequency modulated pattern data from pattern generator 404 via interface 406. Thus, phase shifting is accomplished, suitably via a delay, at the phase shifter 402 in connection with the frequency encoded modulation pattern data.

As far as "Frequency Domain waveform concern, it shapes triangle waveform, means the frequency is sweeping between f0 – 5 x Delta and f0 + 5 x Delta. From the spectrum view point, it has been split out up to 11 kind of frequencies, such as f0-5xD, f0-4xD, f0-3xD, f0-2xD, f0-1xD, f0, f0+1xD, f0+2xD, f0+3xD, f0+4xD, and f0+5xD.

In Fig. 10, another type of implementation has been described. In this implementation, single non-SSCGed 20 MHz clock is used.

Turning to Fig. 11, disclosed is a sample embodiment of a circuit employing the spread spectrum clock generator of the subject application. A suitable clock signal is provided as an input 500 into a spread spectrum clock generating unit 510. As taught above, a unit 510 includes a delay line 512 adapted to receive pattern output from a pattern generator 514. The pattern generator 514, in turn, is incremented in connection with a counter 516 connected operatively thereto. The counter 516 increments in connection with an input clock signal received on input 500. In the disclosed embodiment, the delay line 512 is comprised of 512 stage lines. The output of the spread spectrum clock generator 510 forms input 520 to a phase lock loop (PLL) 522. In the disclosed embodiment, PLL 522 multiplies the input signal at 520 by 20 times. The resultant 400MHz signal is communicated to a microprocessor 524, to form a clock input to allow the microprocessor to run at its selected rate. The 400 MHz signal also forms an input to dividers 526, 530 and 534 which are, in the disclosed example 1/3, 1/4 and 1/6 dividers. The representative divisions allow for selected clock inputs to be placed into several illustrated components. The 400 MHz signal in the disclosed example, when divided by 3, provides a 133.33 MHz clock signal into DRAM controller 528. The same signal, when divided by 4 at the divider 530, provides a requisite 100 MHz signal to a representative structure of an ATA 100 MHz interface. Finally, the divide by 6 divider 534 provides a requisite 33.33 MHz to the illustrated PCI interface.

Thus, it would be appreciated by a review of the example structure of Fig. 11, the spread spectrum clock generator advantageously provides a means by which a suitable spread spectrum clock signal may be generated to several digital synchronous devices operating at various clock frequencies.

The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of the ordinary skilled in the art to utilize the invention

in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance to the breadth to which they are fairly, legally and equitably entitled.